

Dr. Todd Hubing received a BSEE degree from the Massachusetts Institute of Technology, an MSEE from Purdue University and a PhD (EE) from North Carolina State University. Dr. Hubing is recognized as a leading authority in the advancement and novel application of computational electromagnetics (CEM) for solving real world EMC problems. He began his career more than 20 years ago when he joined the Radiation Engineering Laboratory at IBM in Research Triangle Park. At IBM, he contributed to the development of dozens of new products including networking equipment, communications products, and some of the earlier personal computers.

EMC Tutorial
by
Dr. Todd Hubing



In 1989, Dr. Hubing left IBM to join the University of Missouri – Rolla (UMR) where he was a leader in establishing the UMR EMC Laboratory. The lab became a valuable source for information on CEM. Currently, Dr. Hubing is the Michelin Professor of Vehicle Electronics at Clemson University's International Center for Automotive Research.

The participants will receive from this seminar knowledge necessary to appreciate the study of EMC and how it applies to the design and layout of printed circuit boards.



***This Program will qualify for
.6 Continuing Educational Unit Credits***

Welcome ... from Jim Blaha, EMC Chapter Chairperson



2011 is our 11th year of IEEE EMC Seminar's.

Printed Circuit Board layout is often the single most important factor affecting the EMC of electronic systems. PCB's that are auto-routed or laid out according to a list of "design rules" do not usually meet EMC requirements on the first pass resulting in expensive EMC "fixes" such as ferrites on cables and shielded enclosures. Dr. Todd Hubing has lectured internationally on these design issues. We are very honored to have Dr. Hubing with us as we start another decade of IEEE EMC Seminars. Our Goal of providing EMC Seminars that are **Local, Affordable and Providing the Highest Level of Educational Value** is again accomplished through Dr. Todd Hubing. Our Program Committee invites you to participate in this year's outstanding program.

Printed Circuit Board Layout for EMC Suppression

~~~ Attendance will be Limited to 150 ~~~ Register Early ~~~

7:30 – 8:20am

Registration and Continental Breakfast

8:20 – 8:30am

Welcome and Introductions

8:30 – 10:00am

1st Technical Session

Introduction and Impact of Layout on Product Compliance and Cost

Examples of Good and Bad Board Layouts
Signal Routing and Termination
Tracing Current Paths

10:00 – 10:30am

Morning Refreshment Break

Exhibitors Display and Demonstrations

10:30 – 12:00pm

2nd Technical Session

PCB Grounding, Filtering and Shielding

Ground vs. Signal Return
To-Segment - or - Not-to-Segment Planes
Filters that Work Above 100 MHz
Effective and Ineffective Shielding

12:00 – 1:00pm

**Lunch with the Exhibitors and
IEEE Acknowledgments**

1:00 – 2:30pm

3rd Technical Session

ID - Unintentional Antennas on a PCB

Essential Elements of an Antenna
Cables and Enclosures as Radiating Elements
Board Structures that Potentially Radiate

2:30 – 3:00pm

Afternoon Refreshment Break

Exhibitors Display and Demonstrations

3:00 – 3:15pm

IEEE Recognition Awards

3:15 – 4:45pm

4th Technical Session

Strategies for PCB Layout

Design Guidelines (Good and Bad)
Optimizing Component Placement
Stack-up and Routing Priorities
Common Problems - Easily Avoidable

4:45 – 4:50pm

Mr. Jim Blaha

Closing Comments and Seminar Survey

4:50 – 5:45pm

**Last Chance with Exhibitors
Post Seminar Social**